

# **SOI SUBSTRATE HAVING AN ETCH STOP LAYER, AND FABRICATION METHOD THEREOF, SOI INTEGRATED CIRCUIT FABRICATED THEREON, AND METHOD OF FABRICATING SOI INTEGRATED CIRCUIT USING THE SAME**

## **BACKGROUND OF THE INVENTION**

### Field of the Invention

[0001] The present invention relates to a semiconductor device and to a method of fabricating the same. More particularly, the present invention relates to a silicon-on-insulator (SOI) integrated circuit having an electro-static discharge (ESD) circuit and to a method of fabricating the same.

### Description of the Related Art

[0002] Generally, a semiconductor device includes an electro-static discharge (ESD) circuit for protection. Thus, a semiconductor device can endure several thousand volts applied instantaneously from external sources. The ESD circuit has a function of protecting an internal circuit by bypassing static charges injected into each pad, through a power pad or a ground pad, in the event that a voltage deviating from the range of operating voltage is applied to each pad.

[0003] Problems with silicon substrates, which are widely used as substrates for semiconductor devices, however, can render forming an ESD circuit difficult for reasons that will follow.

[0004] First, forming shallow source/drain regions of a transistor is difficult making it not only difficult to realize highly integrated semiconductor devices, but also to decrease parasitic capacitance between the silicon substrate and the source/drain regions. Consequently, it is difficult to obtain improvements in the operation speed of semiconductor devices. Second, when forming a

semiconductor memory device at a silicon substrate, it is difficult to decrease a soft error rate (SER) due to the cell-formed well. Third, when fabricating a semiconductor device having a CMOS circuit, it is difficult to suppress latch-up phenomenon.

[0005] Recently, in response to the above-mentioned problems associated with forming a semiconductor device at a silicon substrate, a technique of fabricating a semiconductor integrated circuit at a SOI substrate has been widely used. However, there are still limitations on the formation of an ESD circuit when fabricating a semiconductor device at a SOI substrate

[0006] Fig. 1 illustrates an equivalent circuit design of a typical SOI integrated circuit having an ESD circuit.

[0007] Referring to Fig. 1, an input pad 50 is connected with an internal circuit 100 through an ESD circuit 1. The ESD circuit 1 includes a diode D. The ESD circuit 1 may also include a MOS transistor. A n-type region and a p-type region of the diode are connected with the input pad 50 and a ground terminal, respectively. Also, the input pad 50 is connected with an input terminal of the internal circuit 100. The input terminal of the internal circuit 100 corresponds to a gate electrode of the MOS transistor composing a CMOS circuit. Although an inverter including both a PMOS transistor  $T_p$  and an NMOS transistor  $T_n$  is given here as an example of the internal circuit, the internal circuit may be a circuit including a NAND gate, a NOR gate or a combination thereof.

[0008] Reverse bias breakdown voltage of the diode D should be higher than the operating voltage of the internal circuit 100, that is, power voltage. Also,

reverse bias breakdown voltage of the diode D should be lower than the gate oxide layer breakdown voltage of both the PMOS transistor Tp and the NMOS transistor Tn composing the internal circuit 100.

[0009] When applying voltage higher than the reverse bias breakdown voltage of the diode D to the input pad 50, a large current is by-passed to the ground terminal through the diode D. Thus, although a high voltage of several thousand volts is applied to the input pad 50, a voltage, which is applied to the input terminal of the internal circuit, is higher than the power voltage and lower than the gate oxide layer breakdown voltage. Thus, the internal circuit 100 is protected by the ESD circuit 1.

[0010] Figs. 2 through 4 illustrate cross-sectional views of a conventional fabrication method for realizing the SOI integrated circuit shown in Fig. 1.

[0011] Referring to Fig. 2, a SOI substrate is prepared. The SOI substrate includes a supporting substrate 11, a buried oxide layer 13 stacked on the supporting substrate 11 and a semiconductor layer 15 stacked on the buried oxide layer 13. A device isolation layer 15a is selectively formed at a predetermined region of the semiconductor layer 15. The device isolation layer 15a is formed to contact with the buried oxide layer 13. Thus, active regions 15b surrounded by the device isolation layer 15a and the buried oxide layer 13 are defined. A photoresist pattern 17 is formed on the resultant structure where the device isolation layer 15a is formed. The photoresist pattern 17 has a first opening 17a and a second opening 17b exposing predetermined regions of the ESD circuit region 1.

[0012] Referring to Fig. 3, the device isolation layer 15a and the buried oxide layer 13 are continuously dry-etched using the photoresist pattern 17 of Fig. 2 as an etch mask, to form holes exposing predetermined regions of the supporting substrate 11. At this time, the exposed supporting substrate 11 has a damaged surface 21 resulting from the dry-etch. Epitaxial layers are selectively formed on the damaged surface 21. Thus, because a property of the semiconductor epitaxial layers is that they are directly affected by the underlying layer, first and second semiconductor epitaxial layers 19a and 19b have crystalline defects.

[0013] Referring to Fig. 4, the NMOS transistor T<sub>n</sub> and the PMOS transistor T<sub>p</sub> of Fig. 1 are formed at the active regions 15b in the internal circuit region 100 using a conventional method. The NMOS transistor includes both a gate oxide layer 21 and a first gate electrode 23<sub>n</sub> sequentially stacked on a predetermined region of the active region 15b. Further, the NMOS transistor includes a first source region 27<sub>s</sub> and a first drain region 27<sub>d</sub> formed at both sides of the first gate electrode 23<sub>n</sub>, respectively. Likewise, the PMOS transistor includes a gate oxide layer 21 and a second gate electrode 23<sub>p</sub> sequentially stacked on a predetermined region of the active region adjacent to the NMOS transistor. The PMOS transistor also includes a second source region 29<sub>s</sub> and a second drain region 29<sub>d</sub> formed at both sides of the second gate electrode 23<sub>p</sub>, respectively.

[0014] Further, spacers 25 are formed on sidewalls of the first and second gate electrodes 23<sub>n</sub> and 23<sub>p</sub>. Also, metal silicide layers 31 may be formed on the first and second gate electrodes 23<sub>n</sub> and 23<sub>p</sub>, and the first and

second source/drain regions 27s, 27d, 29s and 29d, through a self-aligned silicide (salicide) process.

[0015]           Meanwhile, a p-type impurity layer 29p and an n-type impurity layer 27p are formed in the first and second semiconductor epitaxial layers 19a and 19b of Fig. 3, respectively. The n-type impurity layer 27p may be formed simultaneously with the first source/drain regions 27s and 27d, and the p-type impurity layer 29p may be formed simultaneously with the second source/drain region 29s and 29d. Also, the metal silicide layers 31 may be formed even at the surfaces of the n-type and p-type impurity layers 27p and 29p. The n-type and p-type impurity layers 27p and 29p correspond to the n-type and p-type regions of the diode D illustrated in Fig. 1, respectively. Consequently, a junction of the diode D exists in the semiconductor epitaxial layers 19a and 19b, and thus, the diode shows a very inferior leakage current characteristic.

[0016]           According to the conventional technology as described above, the leakage current characteristic of the diode used as the ESD circuit becomes remarkably lowered. Thus, the ESD characteristic of the SOI integrated circuit is degraded.

#### **SUMMARY OF THE INVENTION**

[0017]           It is therefore a feature of an embodiment of the present invention to provide a SOI substrate having an etch stopping layer interposed between a buried oxide layer and a supporting substrate.

[0018]           It is another feature of an embodiment of the present invention to provide a SOI integrated circuit having an improved ESD characteristic by

forming an ESD diode without crystalline defects at a SOI substrate having an etch stopping layer that is interposed between a buried oxide layer and a supporting substrate.

[0019] It is still another feature of an embodiment of the present invention to provide a method of fabricating a SOI substrate having an etch stopping layer interposed between a buried oxide layer and a supporting substrate.

[0020] Further, it is another feature of an embodiment of the present invention to provide a method of fabricating a SOI integrated circuit that can improve an ESD characteristic using a SOI substrate having an etch stopping layer interposed between a buried oxide layer and a supporting substrate.

[0021] A feature of an embodiment of the present invention may be addressed by a SOI integrated circuit according to the present invention. The SOI substrate includes an etch stopping layer, a buried oxide layer and a semiconductor layer sequentially formed on a front surface of a supporting substrate.

[0022] Preferably, the supporting substrate is a single crystalline semiconductor substrate such as a single crystalline silicon substrate. Also, it is preferable that the etch stopping layer is an insulation layer having an etch selectivity with respect to the buried oxide layer, i.e., a silicon nitride layer. The SOI substrate may further comprise a buffer oxide layer interposed between the supporting substrate and the etch stopping layer.

[0023] Another feature of an embodiment of the present invention may be addressed by a SOI integrated circuit in accordance with the present

invention. The SOI integrated circuit includes a SOI substrate. The SOI substrate includes a supporting substrate of a first conductivity type, an etch stopping layer stacked on the supporting substrate, a buried oxide layer stacked on the etch stopping layer, and a semiconductor layer stacked on the buried oxide layer. Device isolation layers are preferably formed at predetermined regions of the semiconductor layer to define first and second active regions. The supporting substrate preferably contacts with first and second semiconductor epitaxial layers that pierce the device isolation layer, the buried oxide layer and the etch stopping layer. A pick-up region of the first conductivity type and another pick-up region of the second conductivity type are preferably disposed at surfaces of the first and second semiconductor epitaxial layers, respectively. The first and second conductivity types may correspond to a p-type and an n-type, respectively, or vice versa. NMOS and PMOS transistors are preferably formed at the first and second active regions, respectively. Here, the pick-up regions and the supporting substrate compose the diode of the ESD circuit.

[0024] The pick-up regions, the device isolation layer, the NMOS and PMOS transistors are preferably covered with an interlayer insulation layer. First and second interconnections and an input pad may be disposed on the interlayer insulation layer. In the event that the first and second conductivity types are p-type and n-type, respectively, the first interconnection is electrically connected with the pick-up region of the first conductivity type and the second interconnection is electrically connected with the pick-up region of the second conductivity type and the input pad. Further, the

second interconnection is connected with the input terminal of a CMOS internal circuit including the NMOS transistor and the PMOS transistor.

[0025] A buffer oxide layer may also be interposed between the supporting substrate of the first conductivity type and the etch stopping layer. In this case, the first and second semiconductor epitaxial layers pierce the buffer oxide layer.

[0026] Another feature by an embodiment of the present invention may be addressed by a method of fabricating a SOI substrate in accordance with the present invention. The method includes forming first and second semiconductor layers and a buried oxide layer in sequence on a front surface of a semiconductor substrate, and forming an etch stopping layer on a front surface of a supporting substrate. It is preferable that the supporting substrate is a single crystalline semiconductor substrate such as a single crystalline silicon substrate. The etch stopping layer and the buried oxide layer are contacted with each other to bond the semiconductor substrate to the supporting substrate. The semiconductor substrate and the first semiconductor layer are selectively removed to expose the second semiconductor layer.

[0027] Preferably, the first semiconductor layer is a porous semiconductor epitaxial layer. Alternatively, the first semiconductor layer may be formed of a bubble layer. Also, the etch stopping layer is preferably formed of an insulation layer such as a silicon nitride layer having an etch selectivity with respect to a silicon oxide layer.



[0028] Yet another feature of an embodiment of the present invention may be addressed by a method of fabricating a SOI integrated circuit in accordance with the present invention. The method includes providing a SOI substrate having a supporting substrate of a first conductivity type, an etch stopping layer stacked on the supporting substrate, a buried oxide layer stacked on the etch stopping layer, and a semiconductor layer stacked on the buried oxide layer. A device isolation layer is formed at a predetermined region of the semiconductor layer to define first and second active regions. The device isolation layer and the buried oxide layer are continuously dry-etched to form first and second preliminary holes exposing the etch stopping layer. The etch stopping layer exposed by the first and second preliminary holes is wet-etched to form first and second holes exposing the supporting substrate. Thus, etch damage applied to the surface of the exposed supporting substrate may be minimized. First and second semiconductor epitaxial layers are grown in the first and second holes, respectively. At this time, growth rates and properties of the first and second semiconductor epitaxial layers are directly affected by the surface state of the exposed supporting substrate. Consequently, in the event that the supporting substrate is a single crystalline semiconductor substrate and there is no etch damage on the surface of the supporting substrate, the first and second semiconductor epitaxial layers also do not have a crystalline defect but a single crystalline structure.

[0029] A pick-up region of a first conductivity type and another pick-up region of a second conductivity type are formed at surfaces of the first and second

semiconductor epitaxial layers, respectively. Also, NMOS and PMOS transistors are formed at the first and second active regions, respectively. In the event that the first and second conductivity types are p-type and n-type, respectively, the pick-up region of the first conductivity type is preferably formed simultaneously with the source/drain regions of the PMOS transistor, and the pick-up region of the second conductivity type is preferably formed simultaneously with the source/drain regions of the NMOS transistor. On the other hand, in the event that the first and second conductivity types are n-type and p-type, respectively, the pick-up region of the first conductivity type is preferably formed simultaneously with the source/drain regions of the NMOS transistor, and the pick-up region of the second conductivity type is preferably formed simultaneously with the source/drain regions of the PMOS transistor.

[0030] Another feature of an embodiment of the present invention may be addressed by a method of fabricating a SOI integrated circuit according to the present invention. The method includes providing a SOI substrate including a supporting substrate of a first conductivity type, an etch stopping layer stacked on the supporting substrate, a buried oxide layer stacked on the etch stopping layer, and a semiconductor layer stacked on the buried oxide layer. A device isolation layer is formed at a predetermined region of the semiconductor layer to define first and second active regions. Then, the device isolation layer and the buried oxide layer are continuously dry-etched to form first and second preliminary holes exposing the etch stopping layer. A pick-up region of a first conductivity type is formed at the supporting

substrate below the etch stopping layer exposed by the first preliminary hole. A pick-up region of a second conductivity type is formed at the supporting substrate below the etch stopping layer exposed by the second preliminary hole. Also, NMOS and PMOS transistors are formed at the first and second active regions, respectively.

[0031] The pick-up region of the first conductivity type is preferably formed by implanting impurity ions of the first conductivity type into the support substrate using the etch stopping layer as a screen material layer. Likewise, the pick-up region of the second conductivity type is preferably formed by implanting impurity ions of the second conductivity type into the support substrate using the etch stopping layer as a screen material layer.

[0032] These and other features and aspects of the present invention will be readily apparent to those of ordinary skill in the art upon review of the detailed description that follows.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0033] Fig. 1 illustrates a partial equivalent circuit diagram of a typical SOI integrated circuit having an ESD circuit.

[0034] Figs. 2 through 4 illustrate cross-sectional views of a method of fabricating a SOI integrated circuit in accordance with a conventional technology.

[0035] Figs. 5 through 13 illustrate cross-sectional views of both a method of fabricating a SOI integrated circuit in accordance with one preferred embodiment of the present invention and the SOI integrated circuit fabricated by the method.

[0036] Figs. 14 through 16 illustrate cross-sectional views of both a method of fabricating a SOI integrated circuit in accordance with another preferred embodiment of the present invention and the SOI integrated circuit fabricated by the method.

#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

[0037] Korean Patent Application No. 2001-28008, filed on May 22, 2001, and entitled: "SOI Substrate having an Etch Stop Layer, and Fabrication Method Thereof, SOI integrated Circuit Fabricated Thereon, and Method of Fabricating SOI Integrated Circuit Using the Same," is incorporated herein by reference in its entirety.

[0038] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the attached figures, the thickness of layers and regions is exaggerated for clarity. Also, when it is mentioned that a layer is on another layer or on a substrate, the layer may be directly formed on another layer or on a substrate, or a third layer may be interposed therebetween. Like reference numbers indicate like components throughout the specification.

[0039] Figs. 5 through 13 illustrate cross-sectional views of methods of fabricating a SOI substrate and a SOI integrated circuit in accordance with a

first preferred embodiment of the present invention. In all figures, parts indicated by the reference numbers "1" and "100" correspond to an ESD circuit region and an internal circuit region, respectively.

[0040] Referring to Fig. 5, a first semiconductor layer 102, a second semiconductor layer 103 and a buried oxide layer 105 are sequentially formed on a front surface of a semiconductor substrate 101 such as a single crystalline silicon substrate. Here, the second semiconductor layer 103 is preferably defined by implanting hydrogen ions into a bulk region of the semiconductor substrate 101 to form the first semiconductor layer 102 composed of a bubble layer at a predetermined depth from the top surface of the semiconductor substrate 101. The method of forming the first and second semiconductor layers 102 and 103 is concretely disclosed in the US. Pat. No. 5,374,564 to Michel Bruel, entitled "Process for the production of thin semiconductor material films," and is omitted here for simplicity.

[0041] Alternatively, the first semiconductor layer 102 may be formed of a porous semiconductor layer. The porous semiconductor layer is formed by anodizing the semiconductor substrate 101. Also, the second semiconductor layer 103 is formed on the porous semiconductor layer using an epitaxial method. At this time, the second semiconductor layer 103 preferably has a higher density than the porous semiconductor layer. The method of forming the porous semiconductor layer and the dense semiconductor epitaxial layer is concretely disclosed in the US. Pat. No. 5,876,497 to Tadashi Atoji, entitled "Fabrication process and fabrication apparatus of SOI substrate," and is omitted here for simplicity.

[0042] The buried oxide layer 105 is formed of a thermal oxide layer or a chemical vapor deposition (CVD) oxide layer. It is desired that the buried oxide layer 105 is formed to a thickness of 1,000Å to 5,000Å.

[0043] Referring to Fig. 6, an etch stopping layer 155 is formed on a front surface of a supporting substrate 151 of a first conductivity type. Here, the first conductivity type corresponds to a p-type. But, the first conductivity type may be an n-type. The etch stopping layer 155 is preferably formed of an insulation layer such as a silicon nitride layer having an etch selectivity with respect to a silicon oxide layer. A buffer oxide layer 153 may be formed on the supporting substrate 151 prior to formation of the etch stopping layer 155. The buffer oxide layer 153 alleviates stress resulting from the difference of the thermal expansion coefficients between the supporting substrate 151 and the etch stopping layer 155. The etch stopping layer 155 and the buffer oxide layer 153 are preferably formed to a relatively thin thickness in comparison with the buried oxide layer 105. For example, the etch stopping layer 155 is preferably formed to a thickness of 100Å to 300Å, and the buffer oxide layer 153 is preferably formed to a thickness of 50Å to 200Å.

[0044] Referring to Fig. 7, a top surface of the buried oxide layer 105 is contacted with a top surface of the etch stopping layer 155 to bond the semiconductor substrate 101 to the supporting substrate 151.

[0045] Referring to Fig. 8, the semiconductor substrate 101 and the first semiconductor layer 102 of Fig. 7 are selectively removed to expose the second semiconductor layer 103. A method of selectively removing the semiconductor substrate 101 and the first semiconductor layer 102 is

concretely disclosed in the US. Pat. No. 5,876,497, and thus, the explanation about the method is omitted for simplicity.

[0046] Here, the supporting substrate 151, the buffer oxide layer 153, the etch stopping layer 155, the buried oxide layer 105 and the second semiconductor layer 103 compose the SOI substrate in accordance with a preferred embodiment of the present invention.

[0047] Referring to Fig. 9, a device isolation layer 103a is formed at a predetermined region of the second semiconductor layer 103 to define multiple active regions 103b such as the first and second active regions in the internal circuit region 100. The device isolation layer 103a contacts with the top surface of the buried oxide layer 105. Thus, sidewalls and bottom surfaces of the first and second active regions 103b are surrounded by the device isolation layer 103a and the buried oxide layer 105. Then, a photoresist pattern 157 having first and second openings 157a and 157b is formed on the semiconductor substrate having the device isolation layer 103a. The first and second openings 157a and 157b expose predetermined regions of the device isolation layer 103a in the ESD circuit region 1.

[0048] Referring to Fig. 10, the device isolation layer 103a and the buried oxide layer 105 are etched using the photoresist pattern 157 as an etch mask to expose predetermined regions of the etch stopping layer 155. At this time, it is desired that the device isolation layer 103a and the buried oxide layer 105 are anisotropically etched using a dry-etch process. Continuously, the exposed etch stopping layer 155 and the underlying buffer oxide layer 153 are wet-etched to form first and second holes 159a and

159b exposing predetermined regions of the supporting substrate 151. Thus, it is possible to prevent the surface of the supporting substrate 151 exposed by the first and second holes 159a and 159b from being etch-damaged. Consequently, the exposed surface of the supporting substrate 151 still has a single crystalline structure. Then, the photoresist pattern 157 is removed.

[0049] Referring to Fig. 11, first and second semiconductor epitaxial layers 161a and 161b are grown in the first and second holes 159a and 159b of Fig. 10 using a conventional selective epitaxial growth process. Here, in the event that the supporting substrate 151 is a single crystalline silicon substrate, the first and second semiconductor epitaxial layers correspond to silicon epitaxial layers having single crystalline structures. Particularly, in the event that there is no crystalline defect at the surface of the exposed supporting substrate 151, the first and second semiconductor epitaxial layers 161a and 161b also have single crystalline structures without crystalline defects. The semiconductor substrate having the first and second semiconductor epitaxial layers 161a and 161b is thermal-oxidized to form a gate insulation layer 163 on the surface of the first and second active regions 103b. At this time, the gate insulation layer 163 is also formed on the surfaces of the first and second semiconductor epitaxial layers 161a and 161b. A conductive layer 165 is formed on the entire surface of the semiconductor substrate including the gate insulation layer 163. The conductive layer 165 is preferably formed of a doped polysilicon layer.

[0050] Referring to Fig. 12, the conductive layer 165 is patterned to form both a first gate electrode 165p crossing over the first active region 103b and



a second gate electrode 165n crossing over the second active region 103b. Then, spacers 167 are formed on the sidewalls of the first and second gate electrodes 165p and 165n, using the conventional method. Also, impurities of a second conductivity type are selectively implanted into the second active region 103b and the second semiconductor epitaxial layer 161b, using the second gate electrode 165n and spacers 167 as ion-implantation masks. Consequently, source/drain regions 169s and 169d of the second conductivity type are formed at the second active region 103b, and at the same time, a pick-up region 169p of the second conductivity type is formed at the second semiconductor epitaxial layer 161b. Likewise, impurities of the first conductivity type are selectively implanted into the first active region 103b and the first semiconductor epitaxial layer 161a, using the first gate electrode 165p and the spacers 167 as ion-implantation masks. Consequently, source/drain regions 171s and 171d of the first conductivity type are formed at the first active region 103b, and at the same time, another pick-up region 171p of the first conductivity type is formed at the first semiconductor epitaxial layer 161a.

[0051] When the first conductivity type is p-type, the second conductivity type corresponds to n-type. On the contrary, when the first conductivity type is n-type, the second conductivity type is p-type. Consequently, in the event that the first and second conductivity types are p-type and n-type, respectively, the PMOS transistor  $T_p$  and the NMOS transistor  $T_n$  of Fig. 1 are formed at the first and second active regions, and p-type and n-type pick-up regions are formed at the first and second semiconductor epitaxial

layers 161a and 161b. Thus, a PN diode D of Fig. 1 is formed in the ESD circuit region 1. The diode is formed at the first and second semiconductor epitaxial layers 161a and 161b without crystalline defects, and thus, has a superior leakage current characteristic in comparison with the conventional technology.

[0052] Referring to Fig. 13, an interlayer insulation layer 175 is formed on the entire surface of the resultant structure where the diode, the NMOS transistor and the PMOS transistor are formed. Before forming the interlayer insulation layer 175, a metal silicide layer 173 may be formed on the pick-up regions 171p and 169p, the first gate electrode 165p, the second gate electrode 165n, and the source/drain regions 169s, 169d, 171s and 171d, using the conventional salicide process.

[0053] The interlayer insulation layer 175 is patterned to form contact holes exposing the metal silicide layer 173. Then, first through fourth interconnections 177g, 177a, 177b, and 177p are formed to cover the contact holes. The first interconnection 177g is electrically connected with the first conductivity type pick-up region 171p and the source region 169s of the NMOS transistor, and the second interconnection 177a is electrically connected with the second conductivity type pick-up region 169p, the first gate electrode 165p and the second gate electrode 165n. Also, the third interconnection 177b is electrically connected with the drain region 169d of the NMOS transistor and the drain region 171d of the PMOS transistor, and the fourth interconnection 177p is electrically connected with the source region 171s of the PMOS transistor.

[0054] In the event that the first and second conductivity types are p-type and n-type, respectively, the first interconnection 177g is connected with a ground line of Fig. 1 and the second interconnection 177a is connected with an input pad 50 of Fig. 1. Further, the fourth interconnection 177p is connected with a power line not shown.

[0055] Consequently, since the diode formed at the ESD circuit region 1 has no crystalline defect, the diode shows a superior junction leakage current characteristic. Therefore, although static charges due to high voltages of several thousand volts are instantly injected into the input pad, the static charges are bypassed to the ground line through the reverse bias current of the diode. Thus, the CMOS circuit in the internal circuit region 100 is protected.

[0056] Figs. 14 through 16 illustrate cross-sectional views of a method of fabricating a SOI integrated circuit in accordance with another preferred embodiment of the present invention.

[0057] Referring to Fig. 14, a SOI substrate having etch stopping layer 155 is formed using a same method as the first preferred embodiment of the present invention. Also, device isolation layer 103a is formed at a predetermined region of the semiconductor layer 103 of the SOI substrate using a same method as the first preferred embodiment of the present invention. Thus, first and second active regions are defined in internal circuit region 100. The device isolation layer 103a and buried oxide layer 105 are continuously anisotropically etched to form first and second preliminary

holes 159c and 159d exposing predetermined regions of the etch stopping layer 155 in ESD circuit region 1.

[0058] Referring to Fig. 15, first conductivity type impurity ions are implanted into the supporting substrate 151 under the first preliminary hole 159c, to form a first conductivity type pick-up region 203. Also, second conductivity type impurity ions are implanted into the supporting substrate 151 of the second preliminary hole 159d, to form a second conductivity type pick-up region 201. Here, the first and second conductivity types may correspond to p-type and n-type, respectively. On the contrary, the first and second conductivity types may correspond to n-type and p-type, respectively. Thus, the PN diode D of Fig. 1 is formed at the supporting substrate 151 in the ESD circuit region 1. Etch stopping layer 155 and buffer oxide layer 153, which exist on the supporting substrate 151, may eliminate etch-damage on the surface of the supporting substrate 151 even though the first and second preliminary holes 159c and 159d are formed using a dry-etch process. Consequently, the diode has a junction without crystalline defects.

[0059] Referring to Fig. 16, PMOS and NMOS transistors are formed at the first and second active regions 103b using a same method as the first preferred embodiment of the present invention. Further, the metal silicide layer 173 may be selectively formed on the gate electrode 165n and source/drain regions 169s and 169d of the NMOS transistor, and on the gate electrode 165p and source/drain regions 171s and 171d of the PMOS transistor. Interlayer insulation layer 175 is formed on the entire surface of the semiconductor substrate including the NMOS and PMOS transistors.

[0060]           Continuously, first through fourth interconnections 177g, 177a, 177b and 177p are formed on the interlayer insulation layer 175 using the same method as the first preferred embodiment of the present invention. Here, the first interconnection 177g is electrically connected with the first conductivity type pick-up region 203 and the source region 169s of the NMOS transistor, and the second interconnection 177a is electrically connected with the second conductivity type pick-up region 201, the first gate electrode 165p and the second gate electrode 165n.

[0061]           Next, referring again to Fig. 8, the SOI substrate in accordance with the present invention will be explained.

[0062]           Referring to Fig. 8, the etch stopping layer 155 is stacked on the supporting substrate 151 of the first conductivity type, which may be p-type or n-type. A top surface of the etch stopping layer 155 is covered with the buried oxide layer 105, and a top surface of the buried oxide layer 105 is covered with the semiconductor layer 103. The buffer oxide layer 153 may be interposed between the etch stopping layer 155 and the supporting substrate 151. It is preferable that the etch stopping layer 155 is an insulation layer such as a silicon nitride layer having an etch selectivity with respect to the buried oxide layer 105. The buffer oxide layer 153 prevents stress due to application of the etch stopping layer to the supporting substrate 151. The supporting substrate 151 includes a single crystalline silicon substrate.

[0063] Referring again to Figs. 13 and 16, the SOI integrated circuits in accordance with the first and second preferred embodiments of the present invention will be explained.

[0064] Referring to Fig. 13, the device isolation layer 103a is disposed at a predetermined region of the semiconductor layer 103 of the SOI substrate illustrated in Fig. 8. The device isolation layer 103a defines the first and second active regions 103b in the internal circuit region 100. The first and second semiconductor epitaxial layers 161a and 161b are located in the first and second holes piercing the device isolation layer 103a, the buried oxide layer 105, the etch stopping layer 155 and the buffer oxide layer 153. The first and second semiconductor epitaxial layers 161a and 161b contact with the supporting substrate 151. The first conductivity type pick-up region 171p is formed at the surface of the first semiconductor epitaxial layer 161a, and the second conductivity type pick-up region 169p is formed at the surface of the second semiconductor epitaxial layer 161b. Consequently, the PN diode is formed in the ESD circuit region 1.

[0065] Also, the PMOS transistor is formed at the first active region 103b, and the NMOS transistor is formed in the second active region 103b. The PMOS transistor includes the first gate electrode 165p and p-type source/drain regions 171s and 171d, and the NMOS transistor includes the second gate electrode 165n and n-type source/drain regions 169s and 169d. The metal silicide layer 173 may also be formed on the surfaces of the first and second gate electrodes 165p and 165n, the p-type source/drain regions 171s and

171d, the n-type source/drain regions 169s and 169d, and the first and second conductivity type pick-up regions 171p and 169p.

[0066] The semiconductor substrate including the first and second conductivity type pick-up regions 171p and 169p, and the PMOS and NMOS transistors is covered with the interlayer insulation layer 175. The first through fourth interconnections 177g, 177a, 177b and 177p are arranged on the interlayer insulation layer 175.

[0067] In the event that the first and second conductivity types are p-type and n-type, respectively, the first interconnection 177g is electrically connected with the first conductivity type pick-up region 171p, the n-type source region 169s and the ground line of Fig. 1, and the second interconnection 177a is electrically connected with the second conductivity type pick-up region 169p, the first gate electrode 165p, the second gate electrode 165n and the input pad 50 of Fig. 1. Further, the third interconnection 177b is electrically connected with the p-type drain region 171d and the n-type drain region 169d, and the fourth interconnection 177p is electrically connected with the p-type source region 171s and the power line not shown.

[0068] Fig. 16 illustrates a cross-sectional view of the SOI integrated circuit in accordance with the second preferred embodiment of the present invention. The internal circuit region 100 of the SOI integrated circuit in accordance with the second preferred embodiment has the same structure as that in accordance with the first preferred embodiment of the present invention. Thus, explanation about the internal circuit region 100 is omitted.

[0069] Referring to Fig. 16, the first and second preliminary holes are positioned to pierce the device isolation layer 103a and the buried oxide layer 105 in the ESD circuit region 1. The first conductivity type pick-up region 203 is formed at the surface of the supporting substrate 151 under the first preliminary hole. Also, the second conductivity type pick-up region 201 is formed at the surface of the supporting substrate under the second preliminary hole. Thus, the PN diode D of Fig. 1 is formed at the supporting substrate 151 in the ESD circuit region 1. The entire surface of the semiconductor substrate having the PN diode is covered with the interlayer insulation layer 175 filling the first and second preliminary holes. The first through fourth interconnections 177g, 177a, 177b and 177p are arranged on the interlayer insulation layer 175 as in the first preferred embodiment of the present invention as explained in the Fig. 13.

[0070] In the event that the first and second conductivity types are p-type and n-type, respectively, the first interconnection 177g is electrically connected with the first conductivity type pick-up region 203, the source region 169s of the NMOS transistor and the ground line of Fig. 1, and the second interconnection 177a is electrically connected with the second conductivity type pick-up region 201, the first gate electrode 165p, the second gate electrode 165n and the input pad 50 of Fig. 1. Further, the third interconnection 177b is electrically connected with the p-type drain region 171d and the n-type drain region 169d, and the fourth interconnection 177p is electrically connected with the p-type source region 171s and the power line not shown.



[0071] According to the present invention as described above, a PN diode used as an ESD circuit is formed at a single crystalline semiconductor epitaxial layer or at a single crystalline supporting substrate without crystalline defects. Thus, it is possible to realize a high performance ESD diode having a superior leakage current characteristic. Consequently, it is possible to improve an ESD characteristic of a SOI integrated circuit.

[0072] Preferred embodiments of the present invention have been disclosed herein and, although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the spirit and scope of the invention as set forth in the following claims.